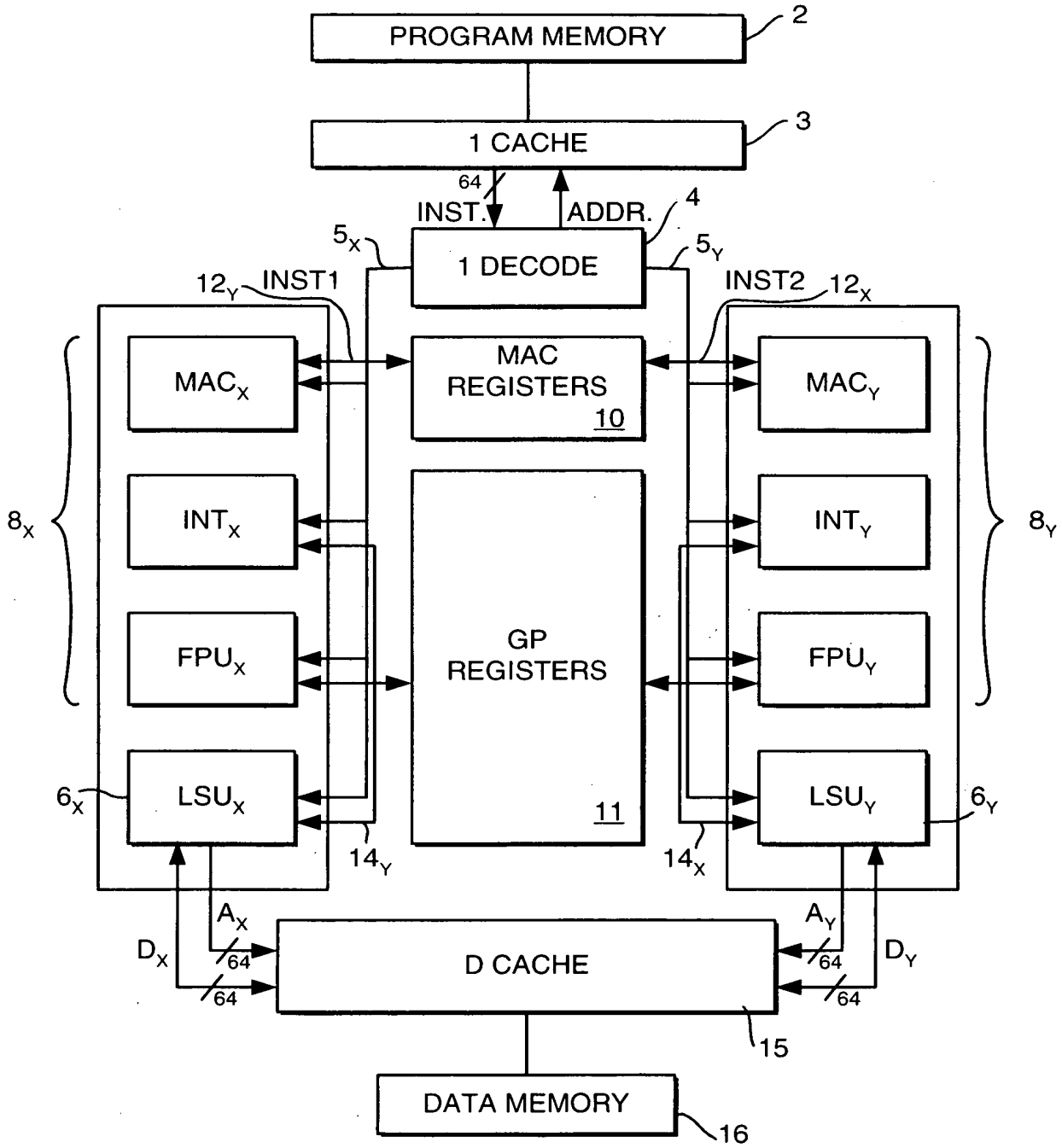
PROGRAM MEMORY
2
1 CACHE
3
64
INST.
ADDR.
4
5X
1 DECODE
5Y
12Y
INST1
INST2
12X
MACX
MAC REGISTERS
10
MACY
8X
INTX
INTY
8Y
FPUX
GP REGISTERS
11
FPUY
6X
LSUX
LSUY
6Y
14Y
14X
AX
AY
DX
64
D CACHE
DY
15
DATA MEMORY
16

FIG. 1

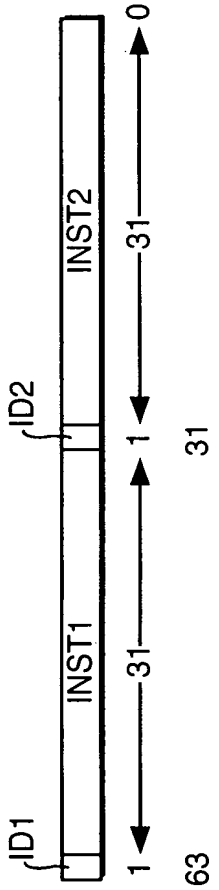

FIG. 2a

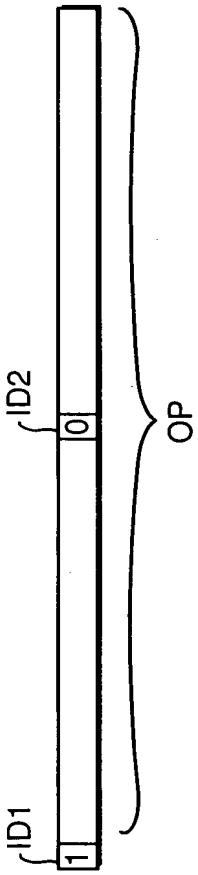

FIG. 2b

IDbit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
M	G	OPCODE					S	TST		SRC2					SRC1					DST											(1)
M	G	OPCODE					TST	IMMED							SRC1					DST											(2)
M	G	OPCODE					S	TST		SRC2					SRC1					SIGN	M REG										(3)
M	G	OPCODE					S	TST		SHIFT	M REG				SRC1					DST											(4)
M	G	OPCODE					S	TST		SRC2					SRC1					DST											(5)
M	OPCODE					T	IMMEDIATE OFFSET								BASE REG					DST											(6)
M	OPCODE					INDX OP			T	INDX REG					BASE REG					DST											(7)

FIG. 3

BIT	31(M)	30(G)	29(G)
REGISTER/ IMMEDIATE	1	0	X
REGISTER/ REGISTER	1	1	0
MAC OPERATIONS	1	1	1

FIG. 4

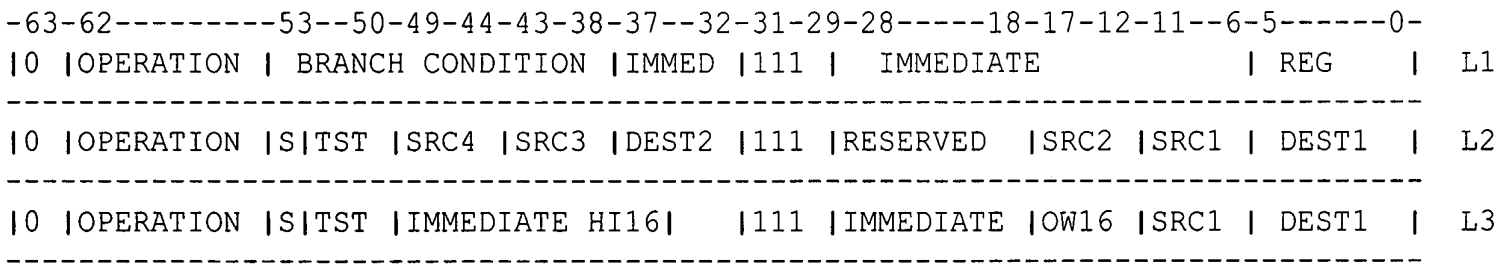

FIG. 5